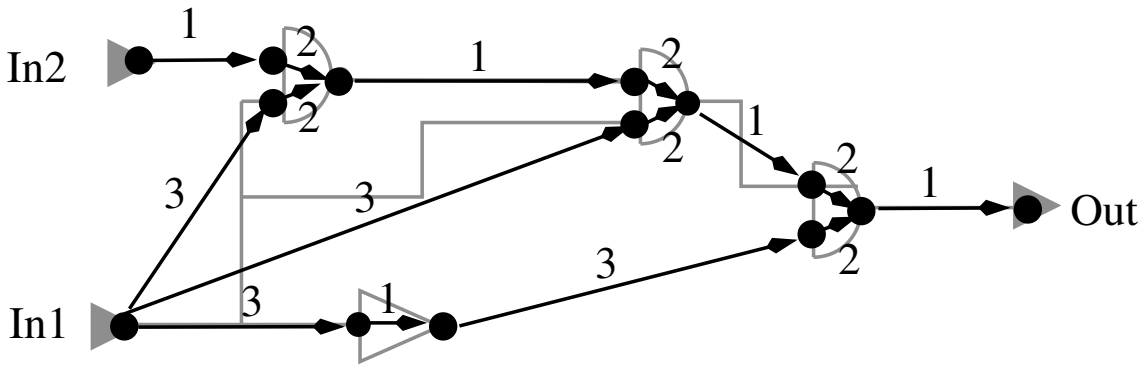
Chip Design
Summer term 2009

Prof. Dr. Jens Vygen
Dr. Stephan Held

Exercises 6

1. Consider following piece of combinatorial logic and its timing graph.



The edge labels specify the delay over the timing graph edge. We do not distinguish between rising and falling signals and do not consider slews/signal shapes. Maximum (late mode) and minimum (early mode) delays are equal. Assume that all the arrival times for the latest and earliest signal at the primary input pins "In1" and "In2" are 0.

What are the earliest and latest arrival times of a signal at the primary output pin "Out"? [2 points]

2. Consider the result of the static timing analysis of a chip.

   Show that the worst late slack $\min\{\overline{\text{slack}}(p,\sigma) \mid \sigma \in S(p)\}$ at a pin p is at least the minimum worst late slack over its predecessors. Show that the same holds for the early slacks. [2 point]

(b) A signal path is a path

$$((v_1,\sigma_1), e_1, (v_2,\sigma_2), e_2, \ldots, (v_n,\sigma_n)),$$

where (v_{i+1},σ_{i+1}) is caused by (v_i,σ_i) by propagation over e_i $(1 \le i < n)$. The late slack of such a path is defined as

$$\overline{\text{rat}}(v_n,\sigma_n) - \overline{\text{at}}(v_1,\sigma_1) - \sum_{i=1}^{n-1} \theta_{e_i}(\overline{\text{shape}}(v_i,\sigma_i)).$$

Assuming delays being invariant in the slews show that the late slack $\overline{\text{slack}}(p, \sigma)$ of a signal $\sigma \in S(p)$ at a node p is the worst (= minimum) late slack of a path through (p, σ).
Formulate and prove an analogous statement for the early slacks. [2 points]

3. Consider a linear optimization problem:

   Problem A:

$$\begin{aligned} \min \;& c_0 + c_1 x_1 + \cdots + c_n x_n \\ s.t. \;& x = (x_1, \ldots, x_n) \in D, \end{aligned}$$

   where $D \subset \mathbb{R}^n$ and $c \in \mathbb{R}^{n+1}$, and the related rational problem on the same solution set:

   Problem B:

$$\begin{aligned} \min \;& \frac{a_0 + a_1 x_1 + \cdots + a_n x_n}{b_0 + b_1 x_1 + \cdots + b_n x_n} \\ s.t. \;& x = (x_1, \ldots, x_n) \in D, \end{aligned}$$

   where $a, b \in \mathbb{R}^{n+1}$ and $b_0 + b_1 x_1 + \cdots + b_n x_n > 0$ for all $x \in D$.

   (a) Show that if Problem A is solvable with $O(p(n))$ comparisons and $O(q(n))$ additions, then Problem B is solvable in time $O(p(n)(q(n)+p(n)))$. (Hint: The algorithm is similar to binary search. Assuming knowledge of the optimum value it runs an algorithm for Problem A for verification and performs a test at every comparison to restrict the optimum solution set.) [8 points]

   (b) Given a digraph G with costs $c : E(G) \to \mathbb{R}$ and weights $w : E(G) \to \mathbb{R}_{\geq 0}$ such that every circuit C in G has positive total weight $w(C) := \sum_{e \in E(C)} w(e) > 0$, show that a circuit C in G with minimum ratio $\frac{c(C)}{w(C)}$ can be determined in strongly polynomial time. [3 points]

   (c) Consider the General Balance Potential Problem for the simplified case that $w(C) > 0$ for all circuits C in G and $|F| = 1$ for all $F \in \mathcal{F}$. Show that this problem can be solved in strongly polynomial time. [3 points]

The deadline for submitting solutions is June 9 before the lecture (12:15).