Chip Design
Summer term 2009

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Exercises 5

1. Consider the Multisection Problem. Let m be the number of regions, $n := |\mathcal{C}|$ the number of circuits, and $S := \max_{C\in\mathcal{C}} \operatorname{size}(C)$. Given a feasible fractional partition g, describe an $O(nm^2)$-time algorithm which finds an integral partition that does not violate any capacity constraint by more than S, and whose cost exceeds the cost of g by at most

$$(m-1)\max_{C\in\mathcal{C}}\max_{1\le i<j\le m} |r(C,i)-r(C,j)|.$$

[5 points]

2. Consider the fractional multisection problem for $m = 2$ regions. Show that there is a simple $O(n \log n)$-time algorithm, not using network flows, which computes an optimum fractional assignment in which all but one circuits are assigned to only one region. [3 points]

3. Consider following specialized legalization problem. A feasible placement consists of integral placement coordinates $x, y : \mathcal{C} \to \mathbb{Z}$ (such that all circuits are located within the chip image), and all circuits have unit height and width. Find a polynomial-time algorithm that, based on an input placement with overlaps, finds a legal placement minimizing the linear or quadratic movement. [3 points]

4. Show that the Single Row Algorithm can be used to minimize the (linear) bounding box netlength, instead of the quadratic movement for the Single Row Placement with Fixed Ordering. (Show how to define the functions f_i.) [4 points]

The deadline for submitting solutions is May 26 before the lecture (12:15).