

Exercise 12

1. The timing constraints of a chip can be modeled by a digraph G with edge delays $d : E(G) \rightarrow \mathbb{R}_+$. The vertices represent the storage elements, the edges represent paths through the combinatorial logic, and the delays are worst-case estimations of the longest propagation time of a signal. An important task is to find an optimum clock schedule, i.e. a mapping $a : V(G) \rightarrow \mathbb{R}$ such that $a(v) + d((v, w)) \leq a(w) + T$ for all $(v, w) \in E(G)$ and a cycle time T that is as small as possible. Show that the problem of finding the numbers $a(v)$ of an optimum solution reduces to the MINIMUM MEAN CYCLE PROBLEM (which is the MINIMUM RATIO CYCLE PROBLEM with unit weights in the denominator). (4 points)
2. Find an instance for the STEINER TREE WITH OPTIMAL ELMORE DELAY PROBLEM for which the Steiner points of any optimum solution are not located on the Hanan-grid. (5 points)
3. Prove Kraft's inequality: Given a finite set S and predefined heights $a_s, s \in S$, there exists a binary tree with the elements of S as the leaves such that each $s \in S$ has depth at most a_s if and only if

$$\sum_{s \in S} 2^{-a_s} \leq 1.$$

(6 points)

4. Show that the variants (a) and (b) of the repeater tree topology generation (pages 91–92 in the script) can be implemented with a running time bound of $O(|S|^2)$. (3 points)

The deadline for this exercise is **Tuesday July 15 at 12:15**, before the lecture.