Chip Design
SS 2008

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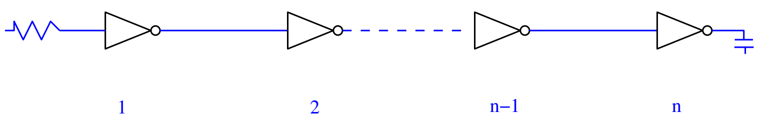
Exercise 10

1. (Enhanced Slew Propagation)
   Consider following modified slew propagation rules:

$$\underline{\text{shape}}(q,\sigma) := \min\left\{\underline{\text{shape}}(e,\sigma) + \nu\cdot(\underline{\text{at}}(e,\sigma) - \underline{\text{at}}(q,\sigma)) \mid e \in \delta^-(q), \sigma \in S(e)\right\},$$
$$\overline{\text{shape}}(q,\sigma) := \max\left\{\overline{\text{shape}}(e,\sigma) + \nu\cdot(\overline{\text{at}}(e,\sigma) - \overline{\text{at}}(q,\sigma)) \mid e \in \delta^-(q), \sigma \in S(e)\right\}$$

   with the notation of the standard slew propagation (pages 75–76 in the script) and a constant $\nu \geq 0$. Let $\hat{\lambda}$ and $\hat{\vartheta}$ be global Lipschitz constants of λ_e and ϑ_e over all $e \in E(G)$ and over the whole range Λ of feasible input slews, i.e. $|\lambda_e(s_1) - \lambda_e(s_2)| \leq \hat{\lambda}|s_1 - s_2|$ and $|\vartheta_e(s_1) - \vartheta_e(s_2)| \leq \hat{\vartheta}|s_1 - s_2|$ for all propagation edges $e \in E(G)$ and all $s_1, s_2 \in \Lambda$. Suppose that $\hat{\lambda} < 1$. Show that using $\nu = \frac{1-\hat{\lambda}}{\hat{\vartheta}}$ leads to arrival time values $\overline{\text{at}}(p,\sigma)$ ($\underline{\text{at}}(p,\sigma)$) for each timing node p and each $\sigma \in S(p)$ that are at least (at most) those of any signal σ propagated to p in full path propagation. Full path propagation is defined as the propagation mode where signals with equal origin and transition are **not** merged, i.e. each path is analyzed independently from others. (6 points)

2. Consider a chain of $n \in \mathbb{N}$ continuously sizable inverters with sizes $x_i \geq L > 0$ ($1 \leq i \leq n$). The $(i+1)$-th inverter is successor of i-th inverter for $1 \leq i < n$.



   Ignore wire delays and assume the RC-delay model from the lecture, i.e. slews and transitions are ignored, and the delay θ_i from the output of inverter $i-1$ to the output of inverter i ($1 \leq i \leq n$) is given by a posynomial

$$\theta_i(x) = \alpha + \frac{\beta}{x_i} C_i$$

   where $x = (x_1, \ldots, x_n)$, $\alpha \geq 0$, $\beta > 0$, and $C_i = x_{i+1}$ for $i = 1, \ldots, n-1$. Furthermore, assume that the start time $\text{at}(0, x)$ of the signal entering the first inverter (inverter 1) depends linearly on the inverter size ($\mathrm{at}(0,x) = \beta x_1$) and that the last inverter drives a fixed capacitance of $C_n = L$.

Derive a closed formula for the size x_i of the $i-th$ inverter in a solution x of the total delay minimization problem:

$$\min\left\{\mathrm{at}(0,x) + \sum_{i=1}^{n} \theta_i(x) \mid x_i \geq L \text{ for all } 1 \leq i \leq n\right\}.$$

(6 points)

The deadline for this exercise is **Tuesday July 1 at 12:15**, before the lecture.