Exercise Set 10

Exercise 10.1:
Show that any instance of the \textit{deadline} version of the \textsc{Discrete Time-Cost Tradeoff Problem} can be transformed into an equivalent instance in which all processing times are positive.

(5 points)

Exercise 10.2:
Consider a chain of \( n \in \mathbb{N} \) continuously sizable inverters with sizes \( x_i > 0 \) (\( 1 \leq i \leq n \)), as in Figure 1.

\begin{center}
\begin{tikzpicture}
  \node at (0,0) (1) {1};
  \node at (1,0) (2) {2};
  \node at (2,0) (n) {n-1};
  \node at (3,0) (n1) {n};
  \draw[->] (1) -- (2);
  \draw[->] (2) -- (n);
  \draw[->] (n) -- (n1);
  \draw[dashed] (n1) -- (n);
\end{tikzpicture}
\end{center}

\textbf{Figure 1}

Assume that the delay \( \theta_i \) through inverter \( i \) is given by

\[ \theta_i(x) = \alpha + \frac{\beta \cdot x_{i+1} + \gamma}{x_i} \quad \text{for} \ 1 \leq i < n - 1 \]

where \( x = (x_1, \ldots, x_n) \), \( \alpha, \gamma \geq 0 \), \( \beta > 0 \). Wire delays, slews and transitions are ignored.

Derive a closed formula for the size \( x_i \) of the \( i \)-th inverter in a solution \( x \) of the total delay minimization problem, assuming \( x_1 \) and \( x_n \) are fixed:

\[ \min \left\{ \sum_{i=1}^{n-1} \theta_i(x) \mid x_i > 0 \text{ for all } 2 \leq i \leq n - 1 \right\} . \]

(5 points)

Exercise 10.3:
Prove Proposition 4.17 from the lecture.

(5 points)
Exercise 10.4:
Consider the netlist shown below in Figure 2. Assume that arrival times at the primary inputs $E_1$ and $E_2$ and required arrival times at the primary outputs $A_1$ and $A_2$ are all identical in each cycle. The latches $Z_1$ and $Z_2$ receive a clock signal once every cycle; this is the latest time when the signal must be stable at the input and the earliest time that the signal at the output can be used. Assume that for each net the delay from the source to any sink is 10 ps, and the circuit delay is 20 ps for all circuits, except for the latches which have no delay and circuit no. 8 whose delay is 40 ps. Determine the maximum possible frequency (i.e. minimum possible cycle time), and the best possible arrival times of the clock signals at the two latches (i.e. a solution of the corresponding instance of the Slack Balancing Problem).

![Figure 2](image-url)

Deadline: July 7th, before the lecture. The websites for lecture and exercises can be found at

[http://www.or.uni-bonn.de/lectures/ss16/ss16.html](http://www.or.uni-bonn.de/lectures/ss16/ss16.html)

In case of any questions feel free to contact me at saccardi@or.uni-bonn.de.