Chip Design
Summer Term 2016

Prof. Dr. Jens Vygen
Pietro Saccardi, M.Sc.

Exercise Set 2

Exercise 2.1:

Let $\mathcal{N}$ be a fully routed netlist. For $N \in \mathcal{N}$, denote with $\mathcal{S}(N)$ the set of all shapes corresponding to the wiring edges of the route of N, and assume that $|\mathcal{S}(N)| \leq k$ for some constant $k \in \mathbb{N}$. Let n be the total number of shapes in $\mathcal{S} := \bigcup_{N \in \mathcal{N}} \mathcal{S}(N)$; each shape is a planar rectangle, with integral coordinates, contained in a chip layer, i.e. each $s \in \mathcal{S}(N)$ is $s = [x_1, x_2] \times [y_1, y_2] \times \{z\}$.

Definition. *Let* $s = [x_1, x_2] \times [y_1, y_2] \times \{z\} \in \mathcal{S}(N)$, $N \in \mathcal{N}$. *Define:*

$$\text{width}(s) := \min\{|x_2 - x_1|, |y_2 - y_1|\}.$$

For another shape $s' = [x_1', x_2'] \times [y_1', y_2'] \times \{z'\} \in \mathcal{S}(N')$, $N \neq N' \in \mathcal{N}$, *define:*

$$\text{dist}(s, s') := \begin{cases} \infty & \text{if } z \neq z' \\ \max\{x_1 - x_2', x_1' - x_2, y_1 - y_2', y_1' - y_2\} & \text{if } z = z'. \end{cases}$$

Formulate a $O(n \log n)$-time algorithm that decides whether the following rules are violated or not:

  (a) *Min distance:* $\text{dist}(s, s') \geq d_0$ for all $s \in \mathcal{S}(N)$, $s' \in \mathcal{S}(N')$, $N, N' \in \mathcal{N}$, such that $N \neq N'$, for a constant $d_0 \in \mathbb{N}$.

  (b) *Min area:* $\text{width}(s \cap s') \geq w_0$ for all $s, s' \in \mathcal{S}(N)$, $N \in \mathcal{N}$ such that $s \cap s' \neq \emptyset$, for a constant $w_0 \in \mathbb{N}$. Note that this implies, in particular, $\text{width}(s) \geq w_0 \; \forall s \in \mathcal{S}(N)$.

(7 points)

Figure 1: The edge labels specify the delays.
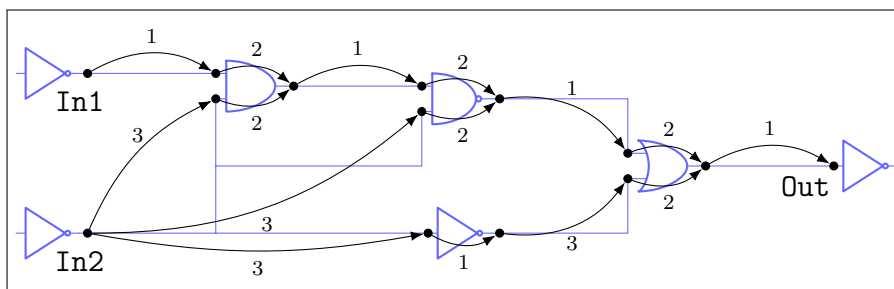
Exercise 2.2:
Consider the piece of combinational logic depicted in Figure 1 and its netlist graph. We do not distinguish between rising and falling signals and do not consider slew. Maximum (late mode) and minimum (early mode) delays are equal. Assume that all the arrival times for the latest and earliest signal at the primary inputs `In1` and `In2` are 0 and the required arrival times at the primary output `Out` are 10 (early mode) and 12 (late mode).

  (a) What are the earliest and latest arrival times at the primary output?
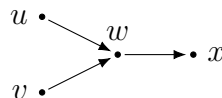 (b) Compute the early and late slack at each pin.

(3 points)

Exercise 2.3:
Prove Proposition 1.6 for $\eta = $ early:

Proposition. *Let p be a pin which is not a logical sink and q a pin which is not a logical source. Let $\eta = $ early. Then*

$$\text{slack}^\eta(p) \geq \min\{\text{slack}^\eta(q) : (p,q) \in \delta^+(p)\};$$
$$\text{slack}^\eta(q) \geq \min\{\text{slack}^\eta(p) : (p,q) \in \delta^-(p)\}.$$

(3 points)

Exercise 2.4:

Consider the timing graph in the figure above. Assume that each primary input u, v has a single signal $(a_u, s_u), (a_v, s_v)$, and that we use enhanced slew propagation in mode $\eta = $ late (the two signals are thus merged into one at w). Let $\text{rat}^\eta(x)$ be fixed, as well as the signal at v and the slew at u. The conditions of Theorem 1.5 hold. Consider $h(a_u) = \text{slack}^\eta(w)$ as a function of a_u. Prove or disprove: $h(a_u)$ is non-increasing.

(7 points)

Deadline: April 28$^{\text{th}}$, before the lecture. The websites for lecture and exercises can be found at

http://www.or.uni-bonn.de/lectures/ss16/ss16.html

In case of any questions feel free to contact me at saccardi@or.uni-bonn.de.