Chip Design
Summer term 2015

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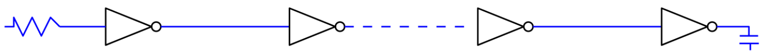
Exercise Set 10

Exercise 10.1:
Consider a chain of $n \in \mathbb{N}$ continuously sizable inverters with sizes $x_i > 0$ ($1 \le i \le n$). The $(i+1)$-th inverter is the successor of the i-th inverter for $1 \le i < n$.



Assume that the delay θ_i through inverter i is given by

$$\theta_i(x) = \alpha + \frac{\beta \cdot x_{i+1} + \gamma}{x_i} \quad \text{for } 1 \le i < n$$
$$\theta_n(x) = \alpha + \frac{\beta \cdot \delta + \gamma}{x_n}$$

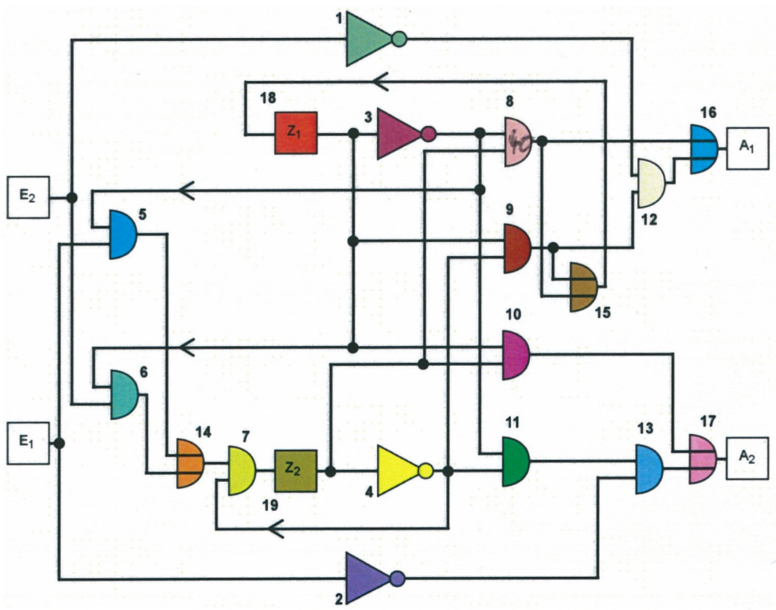
where $x = (x_1, \ldots, x_n)$, $\alpha, \gamma \ge 0$, $\beta, \delta > 0$. Wire delays, slews and transitions are ignored. Furthermore, assume that the start time of the signal entering the first inverter (inverter 1) is given by βx_1.
Derive a closed formula for the size x_i of the $i-th$ inverter in a solution x of the total delay minimization problem:

$$\min \left\{ \beta x_1 + \sum_{i=1}^{n} \theta_i(x) \mid x_i > 0 \text{ for all } 1 \le i \le n \right\}.$$

(5 points)

Exercise 10.2:
Consider the netlist shown below. Assume that arrival times at the primary inputs E_1 and E_2 and required arrival times at the primary outputs A_1 and A_2 are all identical in each cycle. The latches Z_1 and Z_2 receive a clock signal once every cycle; this is the latest time when the signal must be stable at the input and the earliest time that the signal at the output can be used. Assume that for each net the delay from the source to any sink is 10 ps, and the circuit delay is 20 ps for all circuits, except for the latches which have no delay and circuit no. 8 whose delay is 40 ps. Determine the maximum possible frequency (i.e., minimum possible cycle time), and the best possible arrival times of the clock signals at the two latches (i.e., a solution of the corresponding instance of the SLACK BALANCING PROBLEM).

(4 points)



Exercise 10.3:

Let G be an acyclic, directed graph and let $s_1, s_2, t_1, t_2 \in V(G)$ be pairwise distinct vertices. We want to compute a s_1-t_1 path P_1 and a s_2-t_2 path P_2 in G such that P_1 and P_2 are vertex (resp. edge) disjoint or decide that such paths do not exist. Show:

(a) The vertex disjoint and the edge disjoint version are polynomially equivalent.

(b) The vertex disjoint version can be solved in $\mathcal{O}(|V(G)| \cdot |E(G)|)$ time.

(3+5 points)

Exercise 10.4:

In the ESCAPE ROUTING PROBLEM we are given a complete 2-dimensional grid graph G (i.e. $V(G) = \{0, \dots, k-1\} \times \{0, \dots, k-1\}$ and $E(G) = \{\{v, w\} | v, w \in V, \|v - w\| = 1\}$) and a set of pins $P = \{p_1, \dots, p_m\} \subseteq V(G)$. The task is to compute a set of vertex-disjoint paths $\{q_1, \dots, q_m\}$ such that for $i \in \{1, \dots, m\}$ the path q_i connects p_i with a point at the border $B = \{(x, y) \in V(G) | x \in \{0, k-1\} \text{ or } y \in \{0, k-1\}\}$.
Find a polynomial-time algorithm for the ESCAPE ROUTING PROBLEM or prove that the problem is NP-hard.

(3 points)

Deadline: Thursday, July 2nd, before the lecture.

The websites for lecture and exercises are linked at

http://www.or.uni-bonn.de/lectures/ss15/ss15.html

In case of any questions feel free to contact me at ahrens@or.uni-bonn.de.