Chip Design
Summer term 2015

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Exercise Set 2

Exercise 2.1:

Given a netlist with placement and routing. For a net N let $\mathcal{S}(N)$ be the set of all shapes corresponding to the wiring edges of the connection for N. We assume that $|\mathcal{S}(N)| \leq k$ holds for every net N, where $k \in \mathbb{N}$ is a constant.

The routing has to satisfy the following minimum distance rule for a given constant $c \in \mathbb{R}_{>0}$. For any two nets N, N' (with $N \neq N'$) and any pair of shapes $[x_1, x_2] \times [y_1, y_2] \times \{z\} \in \mathcal{S}(N)$ and $[x'_1, x'_2] \times [y'_1, y'_2] \times \{z'\} \in \mathcal{S}(N')$:

$$z \neq z' \text{ or } \max\{x'_1 - x_2, x_1 - x'_2, y'_1 - y_2, y_1 - y'_2\} \geq c. \tag{1}$$

Formulate an $O(n \log n)$-time algorithm that tells whether there is a pair of shapes violating the minimum distance rule. Here n denotes the total number of shapes.

(5 points)

Exercise 2.2:

Construct a family $(G_f)_{f \in \mathcal{F}}$ of directed, acyclic graphs with $s, t \in V(G_f)$ such the number of paths from s to t grows exponentially with the number of edges $|E(G_f)|$.

Remark: This can be used to show that the total number of signals arising in full propagation can depend exponentially on the number of edges in the fine timing graph.

(2 points)

Exercise 2.3:

Prove **Proposition 1.6** for $\eta =$ early:

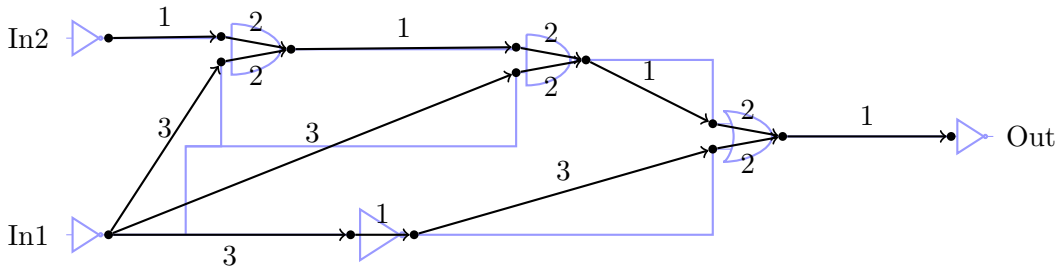
Let p be a pin which is not a logical sink and q a pin which is not a logical source. Then

$$\text{slack}^{\text{early}}(p) \geq \min\{\text{slack}^{\text{early}}(q) \mid (p, q) \in \delta^+(p)\} \text{ and}$$
$$\text{slack}^{\text{early}}(q) \geq \min\{\text{slack}^{\text{early}}(p) \mid (p, q) \in \delta^-(q)\}$$

(3 points)

Exercise 2.4:

Consider the following piece of combinational logic and its netlist graph:



We do not distinguish between rising and falling signals and do not consider slew. Maximum (late mode) and minimum (early mode) delays are equal and shown in the figure. Assume that all the arrival times for the latest and earliest signal at the primary inputs 'In1' and 'In2' are 0 and the required arrival times at the primary output 'Out' are 10 (early mode) and 12 (late mode).

a) What are the earliest and latest arrival times of a signal at the primary output pin?

b) Compute the early and late slack at each pin.

(2 + 3 points)

Exercise 2.5:

Given a connected undirected graph $G = (V, E)$, a set $T \subseteq V$ with $|T| = 3$ and a cost function $c : E \to \mathbb{R}_{\geq 0}$, show how to compute a shortest Steiner tree for T in G in $\mathcal{O}(|V| \log |V| + |E|)$ time.

(5 points)

Deadline: Thursday, April 23rd, before the lecture.

The websites for lecture and exercises are linked at

http://www.or.uni-bonn.de/lectures/ss15/ss15.html

In case of any questions feel free to contact me at ahrens@or.uni-bonn.de.