Chip Design
Summer term 2010

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Exercises 11

1) Given an instance of the Simple Global Routing Problem and additionally a set $\mathcal{P}$ of timing-critical paths with delay bounds $D : \mathcal{P} \to \mathbb{R}_+$. Each path $P \in \mathcal{P}$ consists of a sequence $N_1, N_2, \ldots, N_n$ of nets. Let $\mathcal{Y}_N$ be the set of Steiner trees for $N \in \mathcal{N}$. A delay function $d_N : \mathcal{Y}_N \to \mathbb{R}$ specifies the delay through the circuit driving N. The delay depends on the length of the Steiner tree $Y_N \in \mathcal{Y}_N$ and the additional spacing $s_N(e)$:

$$d_N(Y_N) := \alpha_N + \beta_N \cdot \sum_{e \in E(Y_N)} l(e) \left(w(N,e) + \frac{\zeta_{N,e}}{s_N(e)} \right)$$

with constants $\alpha_N, \beta_N, \zeta_{N,e}$.
We require that

$$\sum_{N \in P} d_N(Y_N) \leq D(P) \text{ for all } P \in \mathcal{P}.$$

Show that the Simple Global Routing Problem with these additional delay constraints can be modeled as a Resource Sharing Problem.

(4 points)

2) Let $\mathcal{C}$ and $\mathcal{B}_c$ ($c \in \mathcal{C}$) be finite sets and $x_{c,b} \geq 0$ for all $c \in \mathcal{C}$ and $b \in \mathcal{B}_c$ with $\sum_{b \in \mathcal{B}_c} x_{c,b} = 1$ for all $c \in \mathcal{C}$. Let $g_c(b) \in \mathbb{R}_+$ for $b \in \mathcal{B}_c$ and $c \in \mathcal{C}$, and $\lambda := \max_{r \in \mathcal{R}} \sum_{c \in \mathcal{C}} \sum_{b \in \mathcal{B}_c} x_{c,b} (g_c(b))_r$.
For $r \in \mathcal{R}$ let $\rho_r := \max\{(g_c(b))_r / \lambda : b \in \mathcal{B}_c, c \in \mathcal{C}, x_{c,b} > 0\}$ and let $\delta > 0$ so that $1 - \sum_{r \in \mathcal{R}} e^{-h(\delta)/\rho_r} > 0$, where $h(\delta) := (1+\delta)\ln(1+\delta) - \delta$.
Show that there is a *deterministic* algorithm that computes $\hat{b}_c \in \mathcal{B}_c$ for $c \in \mathcal{C}$ so that $\hat{\lambda} := \max_{r \in \mathcal{R}} \sum_{c \in \mathcal{C}} (g_c(\hat{b}_c))_r \leq \lambda(1+\delta)$.
Hints: Define for any feasible solution $\hat{x}$:

$$\Psi(\hat{x}) := \sum_{r \in \mathcal{R}} \frac{1}{(1+\delta)^{(1+\delta)\lambda}} \prod_{c \in \mathcal{C}} \left(1 + \delta \sum_{b \in \mathcal{B}_c} \hat{x}_{c,b} (g_c(b))_r \right)$$

and show that if $\Psi(\hat{x}) < 1$ then $\max_{r \in \mathcal{R}} \sum_{c \in \mathcal{C}} \sum_{b \in \mathcal{B}_c} \hat{x}_{c,b} (g_c(b))_r \leq \lambda(1+\delta)$.
For $c' \in \mathcal{C}$ consider the solutions $\hat{x}^{c',b'}$ for $b' \in \mathcal{B}_{c'}$ defined by

$$\hat{x}^{c',b'}_{c,b} := \begin{cases} 1 & c = c', b = b', \\ 0 & c = c', b \neq b', \\ x_{c,b} & \text{otherwise.} \end{cases}$$

and compute $\sum_{b' \in \mathcal{B}_{c'}} x_{c',b'} \Psi(\hat{x}^{c',b'})$.

(4 points)

3) When producing the mask of a chip, dust particles might create errors. A dust particle creates an *open* if it covers the complete width of a wire and a *short* if it touches two different wires:

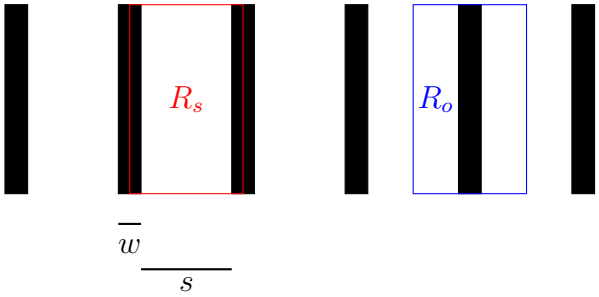
In our model all dust particles are circles with some radius r that are uniformly distributed over the chip area. As probability distribution for r we take $f(r) = \frac{k}{r^3}$ for $r \geq r_0$ where $r_0 \in \mathbb{R}_{r>0}$ is smaller than the smallest radius of a dust particle that might create an error and k is chosen so that $\int_{r_o}^{\infty} f(r)dr = 1$.
For each point (x, y) of an area $[x_1, x_2] \times [y_1, y_2]$ let $t_s(x, y)$ and $t_o(x, y)$ be the minimum size of a particle on position (x, y) such that it produces a short and an open, respectively. The *critical area* with respect to shorts and opens, respectively, is defined as

$$C_{short}([x_1, x_2] \times [y_1, y_2]) := c_s \int_{x\in[x_1,x_2]} \int_{y\in[y_1,y_2]} \int_{t_s(x,y)}^{\infty} f(r)drdydx$$

and

$$C_{open}([x_1, x_2] \times [y_1, y_2]) := c_o \int_{x\in[x_1,x_2]} \int_{y\in[y_1,y_2]} \int_{t_o(x,y)}^{\infty} f(r)drdydx,$$

where $c_s > 0$ and $c_o > 0$ are some constants. (The estimated wiring yield loss depends monotonically on the critical area.)
By allowing extra space for each wire and increasing its width we can reduce the critical area. We model the critical area by a cost function $\gamma_{N,e} : \mathbb{R}_+ \to \mathbb{R}_+$ for each $N \in \mathcal{N}$ and $e \in E(G)$ where $\gamma_{N,e}(s)$ is the estimated contribution if e is used by net N with allocated space $w(N, e) + s$ (see lecture notes page 113).
$\gamma_{N,e}(s)$ is computed the following way. Assume we have a set of parallel vertical wires of width $w := w(N, e)$ and distance s between two neighboring wires. Let R_s and R_o be two axis-parallel rectangles, both of height $l(e)$ and width $w + s$. The corners of R_s are located at the center of a wire and R_o in the middle between two neighboring wires. Then $\gamma_{N,e}(s) := C_{short}(R_s) + C_{open}(R_o)$.



Compute the function $\gamma_{N,e}$ and show that $\gamma_{N,e}$ is convex. (4 points)

Deadline: July 6 before the lecture (12.15 pm).